

**AMENDMENTS TO THE CLAIMS**

This listing of claims will replace all prior listings of claims in the application.

**Listing of Claims:**

1. (Currently Amended) A manufacturing method of a semiconductor wafer, wherein an epitaxial layer (~~17, 27, 37, 47~~) is grown in a trench (~~16, 26, 36, 46~~) of a semiconductor wafer (~~10, 20, 30, 40~~) having a trench structure by gradually reducing a temperature in a temperature range of 400 to 1150°C or by gradually reducing a temperature and then lowering the temperature at a predetermined speed based on a vapor growth method while supplying a silane gas as a raw material gas, thereby filling the epitaxial layer (~~17, 27, 37, 47~~) in the trench (~~16, 26, 36, 46~~).

2. (Currently Amended) The manufacturing method of a semiconductor wafer according to claim 1, comprising:

a step of forming a first layer (~~11~~) on an inner surface of the trench (~~16~~) of the semiconductor wafer (~~10~~) at a first temperature in the range of 900 to 1150°C by the vapor growth method;

a step of forming a second layer (~~12~~) on a surface of the first layer (~~11~~) in the trench (~~16~~) at a second temperature in the range of 850 to 1100°C lower than the first temperature by the vapor growth method; and

a step of forming a third layer (13) on a surface of the second layer (12) in the trench (16) at a third temperature in the range of 800 to 1050°C lower than the second temperature by the vapor growth method so that the epitaxial layer (17) consisting of the first layer (11), the second layer (12) and the third layer (13) is filled in the trench (16).

3. (Currently Amended) The manufacturing method of a semiconductor wafer according to claim 1, comprising:

a step of forming a first layer (21) on an inner surface of the trench (26) of the semiconductor wafer (20) at a first temperature in the range of 900 to 1150°C by the vapor growth method; a step of forming a second layer (22) on a surface of the first layer (21) in the trench (26) at a second temperature in the range of 850 to 1100°C lower than the first temperature by the vapor growth method; a step of forming a third layer (23) on a surface of the second layer (22) in the trench (26) at a third temperature in the range of 800 to 1050°C lower than the second temperature by the vapor growth method; and a step of forming a fourth layer (24) on a surface of the third layer (23) in the trench (26) at a fourth temperature in the range of 750 to 1000°C lower than the third temperature by the vapor growth method so that the epitaxial layer (27) consisting of the first layer (21), the second layer (22), the third layer (23) and the fourth layer (24) is filled in the trench (26).

4. (Currently Amended) The manufacturing method of a semiconductor wafer according to claim 1, comprising:

a step of forming a first layer (31) on an inner surface of the trench (36) of the semiconductor wafer (30) at a first temperature in the range of 900 to 1150°C by the vapor growth method;

a step of forming a second layer (32) on a surface of the first layer (31) in the trench (36) at a second temperature in the range of 850 to 1100°C lower than the first temperature by the vapor growth method; and

a step for forming a third layer (33) on a surface of the second layer (32) in the trench (36) by the vapor growth method while reducing a temperature from the second temperature at a speed of 1 to 100°C/min so that the epitaxial layer (37) consisting of the first layer (31), the second layer (33) and the third layer (33) is filled in the trench (36).

5. (Currently Amended) The manufacturing method of a semiconductor wafer according to claim 1, comprising:

a step of forming a first layer (41) on an inner surface of the trench (46) of the semiconductor wafer (40) at a first temperature in the range of 900 to 1150°C by the vapor growth method;

a step of forming a second layer (42) on a surface of the first layer (41) in the trench (46) at a second temperature in the range of 850 to 1100°C lower than the first temperature by the vapor growth method;

a step of forming a third layer (43) on a surface of the second layer (42) in the trench (46) at a third temperature in the range of 800 to 1050°C by the vapor growth method; and

a step of forming a fourth layer (44) on a surface of the third layer (43) in the trench (46) by the vapor growth method while reducing a temperature from the third temperature at a speed of 1 to 100°C/min so that the epitaxial layer (47) consisting of the first layer (41), the second layer (42), the third layer (43) and the fourth layer (44) is filled in the trench (46).

6. (Currently Amended) The manufacturing method of a semiconductor wafer according to claim 2, wherein a thickness  $w_1$  of the first layer (11, 31) is  $(W/20) \leq w_1 (W/10)$ , a thickness  $w_2$  of the second layer (12, 32) is  $(W/10) \leq w_2 \leq (W/5)$ , and the remainder is the third layer (13, 33), where  $W$  is a width of the trench (16, 36).

7. (Currently Amended) The manufacturing method of a semiconductor wafer according to claim 3, wherein a thickness  $w_1$  of the first layer (21, 41) is

$(W/20) \leq w_1 \leq (W/10)$ , a thickness  $w_2$  of the second layer ~~(22, 42)~~ is  $(W/10) \leq w_2 \leq (W/5)$ , a thickness  $w_3$  of the third layer ~~(23, 43)~~ is  $(W/10) \leq w_3 \leq (W/5)$   $(W/10) \leq w_3 \leq (W/5)$ , and the remainder is the fourth layer ~~(22, 44)~~, where  $W$  is a width of the trench ~~(26, 46)~~.

8. (Currently Amended) The manufacturing method of a semiconductor wafer according to claim 2, wherein, when the semiconductor wafer ~~(10, 20, 30, 40)~~ is left in the air for eight hours or more in a state where the trench ~~(16, 26, 36, 46)~~ has been formed in the semiconductor wafer ~~(10, 20, 30, 40)~~ or in a state where the first layer ~~(11, 21, 31, 41)~~, the second layer ~~(12, 22, 32, 42)~~ or the third layer ~~(13, 23, 33, 43)~~ has been formed on the inner surface of the trench ~~(16, 26, 36, 46)~~, the semiconductor wafer ~~(10, 20, 30, 40)~~ is dipped in a mixture of an alkaline water solution and hydrogen peroxide solution having an etching rate of 0.1 to 1 nm/min for 1 to 10 minutes and cleansed, and then the semiconductor wafer ~~(10, 20, 30, 40)~~ is dipped in fluorinated acid for 0.1 to 60 minutes and cleansed.

9. (Currently Amended) The manufacturing method of a semiconductor wafer according to claim 8, wherein the semiconductor wafer ~~(10, 20, 30, 40)~~ is dipped in an acidic or alkaline etchant having an etching rate of 0.1 to 1  $\mu\text{m}/\text{min}$  for 0.1 to 10 minutes to increase a width of the trench ~~(16, 26, 36, 46)~~ before forming the third layer ~~(13, 33)~~ or

the fourth layer (~~24, 44~~) required to completely fill the inside of the trench (~~16, 26, 36, 46~~) of the semiconductor wafer (~~10, 20, 30, 40~~).

10. (Original) The manufacturing method of a semiconductor wafer according to claim 1, wherein a temperature at which the epitaxial layer is grown by the vapor growth method falls within a range of 650 to 950°C.

11. (Original) The manufacturing method of a semiconductor wafer according to claim 1, wherein a temperature at which the epitaxial layer is grown by the vapor growth method falls within a range of 400°C to 650°C.

12. (Withdrawn) A semiconductor wafer manufactured by the method defined in claim 1.

13. (Currently Amended) The manufacturing method of a semiconductor wafer according to claim 4, wherein a thickness  $w_1$  of the first layer (~~11, 31~~) is  $(W/20) \leq w_1 \leq (W/10)$ , a thickness  $w_2$  of the second layer (~~12, 32~~) is  $(W/10) \leq w_2 \leq (W/5)$ , and the remainder is the third layer (~~13, 33~~), where  $W$  is a width of the trench (~~16, 36~~).

14. (Currently Amended) The manufacturing method of a semiconductor wafer according to claim 5, wherein a thickness  $w_1$  of the first layer ~~(21, 41)~~ is  $(W/20) \leq w_1 \leq (W/10)$ , a thickness  $w_2$  of the second layer ~~(22, 42)~~ is  $(W/10) \leq w_2 \leq (W/5)$ , a thickness  $w_3$  of the third layer ~~(23, 43)~~ is  $(W/10) \leq w_3 \leq (W/5)$   $(W/10) \leq w_3 \leq (W/5)$ , and the remainder is the fourth layer ~~(22, 44)~~, where  $W$  is a width of the trench ~~(26, 46)~~.

15. (Withdrawn) A semiconductor wafer manufactured by the method defined in claim 2.

16. (Withdrawn) A semiconductor wafer manufactured by the method defined in claim 3.

17. (Withdrawn) A semiconductor wafer manufactured by the method defined in claim 4.

18. (Withdrawn) A semiconductor wafer manufactured by the method defined in claim 5.

19. (Withdrawn) A semiconductor wafer manufactured by the method defined in claim 6.

20. (Withdrawn) A semiconductor wafer manufactured by the method defined in claim 7.

21. (Withdrawn) A semiconductor wafer manufactured by the method defined in claim 8.

22. (Withdrawn) A semiconductor wafer manufactured by the method defined in claim 9.

23. (Withdrawn) A semiconductor wafer manufactured by the method defined in claim 10.

24. (Withdrawn) A semiconductor wafer manufactured by the method defined in claim 11.